## 3.3 V 1:4 AnyLevel<sup>™</sup> Differential Input to LVDS Fanout Buffer/Translator

The NB6N14S is a differential 1:4 Clock or Data Receiver and will accept AnyLevel<sup>™</sup> differential input signals: LVPECL, CML or LVDS. These signals will be translated to LVDS and four identical copies of Clock or Data will be distributed, operating up to 2.0 GHz or 2.5 Gb/s, respectively. As such, the NB6N14S is ideal for SONET, GigE, Fiber Channel, Backplane and other Clock or Data distribution applications.

The NB6N14S has a wide input common mode range from GND + 50 mV to  $V_{CC}$  – 50 mV. Combined with the 50  $\Omega$  internal termination resistors at the inputs, the NB6N14S is ideal for translating a variety of differential or single–ended Clock or Data signals to 350 mV typical LVDS output levels.

The NB6N14S is offered in a small 3 mm x 3 mm 16–QFN package. Application notes, models, and support documentation are available at *www.onsemi.com*.

The NB6N14S is a member of the ECLinPS MAX  $^{\rm \tiny M}$  family of high performance products.

#### Features

- Maximum Input Clock Frequency > 2.0 GHz
- Maximum Input Data Rate > 2.5 Gb/s
- 1 ps Maximum RMS Clock Jitter
- Typically 10 ps Data Dependent Jitter
- 380 ps Typical Propagation Delay
- 120 ps Typical Rise and Fall Times
- V<sub>REF AC</sub> Reference Output
- TIA/EIA 644 Compliant
- Functionally Compatible with Existing 3.3 V LVEL, LVEP, EP, and SG Devices
- These are Pb-Free Devices

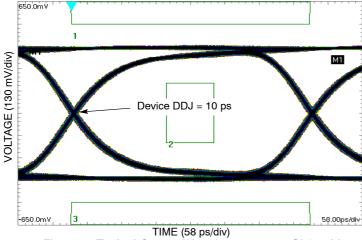
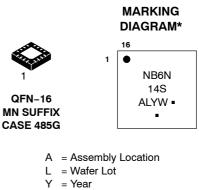


Figure 2. Typical Output Waveform at 2.488 Gb/s with PRBS  $2^{23-1}$  (V<sub>INPP</sub> = 400 mV; Input Signal DDJ = 14 ps)



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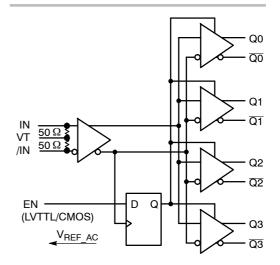


W = Work Week

= Pb-Free Package

(Note: Microdot may be in either location)

\*For additional marking information, refer to Application Note AND8002/D.





#### **ORDERING INFORMATION**

See detailed ordering and shipping information in the package dimensions section on page 10 of this data sheet.

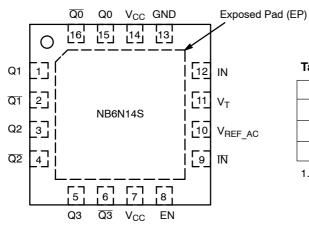


Figure 3. NB6N14S Pinout, 16-pin QFN (Top View)

## Table 1. TRUTH TABLE

IN	ĪN	EN	Q <u>Q</u>	
0	1	1	0	1
1	0	1	1	0
x	х	0	0 (Note 1)	1 (Note 1)

1. On next transition of the input signal (IN).

Table 2. PIN	DESCRIPTION
--------------	-------------

Pin	Name	I/O	Description
1	Q1	LVDS Output	Non–inverted IN output. Typically loaded with 100 $\Omega$ receiver termination resistor across differential pair.
2	Q1	LVDS Output	Inverted IN output. Typically loaded with 100 $\Omega$ receiver termination resistor across differential pair.
3	Q2	LVDS Output	Non-inverted IN output. Typically loaded with 100 $\Omega$ receiver termination resistor across differential pair.
4	Q2	LVDS Output	Inverted IN output. Typically loaded with 100 $\Omega$ receiver termination resistor across differential pair.
5	Q3	LVDS Output	Non–inverted IN output. Typically loaded with 100 $\Omega$ receiver termination resistor across differential pair.
6	<u>Q</u> 3	LVDS Output	Inverted IN output. Typically loaded with 100 $\Omega$ receiver termination resistor across differential pair.
7	V <sub>CC</sub>	-	Positive Supply Voltage.
8	EN	LVTTL / LVCMOS Input	Synchronous Output Enable. When LOW, Q outputs will go LOW and Qb outputs will go HIGH on the next negative transition of IN input. The internal DFF register is clocked on the falling edge of IN input; see Figure 23. The EN pin has an internal pullup resistor and defaults HIGH when left open.
9	ĪN	LVPECL, CML, LVDS	Inverted Differential Input
10	V <sub>REF_AC</sub>	LVPECL Output	The V <sub>REF AC</sub> reference output can be used to rebias capacitor-coupled differential or single-ended input signals. For the capacitor-coupled IN and/or INb inputs, V <sub>REF AC</sub> should be connected to the VT pin and bypassed to ground with a 0.01 $\mu$ F capacitor.
11	V <sub>T</sub>	LVPECL Output	Internal 100 $\Omega$ Center-tapped Termination Pin for IN and $\overline{\text{IN}}$
12	IN	LVPECL, CML, LVDS	Non-inverted Differential Input. (Note 2)
13	GND	-	Negative Supply Voltage.
14	V <sub>CC</sub>	-	Positive Supply Voltage.
15	Q0	LVDS Output	Non-inverted IN output. Typically loaded with 100 $\Omega$ receiver termination resistor across differential pair.
16	<u>Q0</u>	LVDS Output	Inverted IN output. Typically loaded with 100 $\Omega$ receiver termination resistor across differential pair.
-	EP	_	The Exposed Pad (EP) on the QFN-16 package bottom is thermally connected to the die for improved heat transfer out of package. The exposed pad must be attached to a heat-sinking conduit. The pad is not electrically connected to the die, but is recommended to be electrically and thermally connected to GND on the PC board.

 In the differential configuration, when the input termination pin (VT) is connected to a termination voltage or left open, and if no signal is applied on IN/IN inputs, then the device will be susceptible to self-oscillation.

#### Table 3. ATTRIBUTES

Chara	Value	
Moisture Sensitivity (Note 3)		Level 1
Flammability Rating	Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in
ESD Protection Human Body Model Machine Model		> 2 kV > 200 V
Transistor Count	225	
Meets or exceeds JEDEC Sp	ec EIA/JESD78 IC Latchup Test	

3. For additional information, see Application Note AND8003/D.

#### Table 4. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
$V_{CC}$	Positive Power Supply	GND = 0 V		3.8	V
V <sub>IN</sub>	Positive Input	GND = 0 V	$V_{IN} \le V_{CC}$	3.8	V
I <sub>IN</sub>	Input Current Through $R_T$ (50 $\Omega$ Resistor)	Static Surge		35 70	mA mA
I <sub>OSC</sub>	Output Short Circuit Current Line-to-Line (Q to $\overline{Q}$ ) Line-to-End (Q or $\overline{Q}$ to GND) TIA/EIA – 644 Compliant	Q or Q Q to Q to GND	Continuous Continuous	12 24	mA
I <sub>REF_AC</sub>	V <sub>REF_AC</sub> Sink/Source Current			±0.5	mA
T <sub>A</sub>	Operating Temperature Range	QFN-16		-40 to +85	°C
T <sub>stg</sub>	Storage Temperature Range			-65 to +150	°C
$\theta_{JA}$	Thermal Resistance (Junction-to-Ambient) (Note 4)	0 lfpm 500 lfpm	QFN-16 QFN-16	41.6 35.2	°C/W °C/W
$\theta_{\text{JC}}$	Thermal Resistance (Junction-to-Case)	1S2P (Note 4)	QFN-16	4.0	°C/W
T <sub>sol</sub>	Wave Solder Pb-Free			265	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

4. JEDEC standard multilayer board – 1S2P (1 signal, 2 power) with 8 filled thermal vias under exposed pad.

Symbol	Characteristic	Min	Тур	Max	Unit
I <sub>CC</sub>	Power Supply Current (Note 9)		65	100	mA
DIFFERE	TIAL INPUTS DRIVEN SINGLE-ENDED (Figures 14, 15, 19, and 21)				
V <sub>th</sub>	Input Threshold Reference Voltage Range (Note 8)	GND +100		V <sub>CC</sub> – 100	mV
VIH	Single-ended Input HIGH Voltage	V <sub>th</sub> + 100		V <sub>CC</sub>	mV
V <sub>IL</sub>	Single-ended Input LOW Voltage	GND		V <sub>th</sub> – 100	mV
$V_{REF\_AC}$	Reference Output Voltage (Note 11)	V <sub>CC</sub> – 1.600	V <sub>CC</sub> - 1.425	V <sub>CC</sub> - 1.300	V
DIFFERE	TIAL INPUTS DRIVEN DIFFERENTIALLY (Figures 10, 11, 12, 13, 20,	and 22)			
V <sub>IHD</sub>	Differential Input HIGH Voltage	100		V <sub>CC</sub>	mV
V <sub>ILD</sub>	Differential Input LOW Voltage	GND		V <sub>CC</sub> – 100	mV
V <sub>CMR</sub>	Input Common Mode Range (Differential Configuration)	GND + 50		V <sub>CC</sub> – 50	mV
V <sub>ID</sub>	Differential Input Voltage (V <sub>IHD</sub> – V <sub>ILD</sub> )	100		V <sub>CC</sub>	mV
R <sub>TIN</sub>	Internal Input Termination Resistor	40	50	60	Ω
LVDS OU	TPUTS (Note 5)				
V <sub>OD</sub>	Differential Output Voltage	250		450	mV
$\Delta V_{OD}$	Change in Magnitude of V <sub>OD</sub> for Complementary Output States (Note 10)	0	1	25	mV
V <sub>OS</sub>	Offset Voltage (Figure 18)	1125		1375	mV
$\Delta V_{OS}$	Change in Magnitude of $V_{OS}$ for Complementary Output States (Note 10)	0	1	25	mV
V <sub>OH</sub>	Output HIGH Voltage (Note 6)		1425	1600	mV
V <sub>OL</sub>	Output LOW Voltage (Note 7)	900	1075		mV
	CMOS INPUTS	-	-	-	-
VIH	Input HIGH Voltage (Note 7, 8)	2.0		V <sub>CC</sub>	V

V <sub>IH</sub>	Input HIGH Voltage (Note 7, 8)	2.0	V <sub>CC</sub>	V
V <sub>IL</sub>	Input LOW Voltage (Note 7, 8)	GND	0.8	V
I <sub>IH</sub>	Input HIGH Current	-150	150	μA
Ι <sub>ΙL</sub>	Input LOW Current	-150	150	μA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit

values are applied individually under normal operating conditions and not valid simultaneously.

5. LVDS outputs require 100  $\Omega$  receiver termination resistor between differential pair. See Figure 17.

6.  $V_{OH}max = V_{OS}max + \frac{1}{2}V_{OD}max$ . 7.  $V_{OL}max = V_{OS}min - \frac{1}{2}V_{OD}max$ . 8.  $V_{th}$  is applied to the complementary input when operating in single-ended mode.

9. Input termination pins open, D/ $\overline{D}$  at the DC level within V<sub>CMR</sub> and output pins loaded with R<sub>L</sub> = 100  $\Omega$  across differential.

10. Parameter guaranteed by design verification not tested in production.

11. V<sub>REF AC</sub> used to rebias capacitor-coupled inputs only (see Figures 14 and 15).

			-40°C		25°C			85°C			
Symbol	Characteristic	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Unit
f <sub>inMax</sub>	Maximum Input Clock Frequency	2.0			2.0			2.0			GHz
V <sub>OUTPP</sub>	$\begin{array}{l} \mbox{Output Voltage Amplitude (@ V_{INPPmin})} \ f_{in} \leq 1.0 \ GHz \\ (Figure 4) \ f_{in} = 1.5 \ GHz \\ f_{in} = 2.0 \ GHz \end{array}$	220 200 170	350 300 270		220 200 170	350 300 270		220 200 170	350 300 270		mV
f <sub>DATA</sub>	Maximum Operating Data Rate	1.5	2.5		1.5	2.5		1.5	2.5		Gb/s
t <sub>PLH</sub> , t <sub>PHL</sub>	Differential Input to Differential Output Propagation Delay	300	450	600	300	450	600	300	450	600	ps
t <sub>s</sub> t <sub>h</sub>	Setup Time Hold Time	300 500	60 70		300 500	60 70		300 500	60 70		
t <sub>SKEW</sub>	Within Device Skew (Note 17) Device-to-Device Skew (Note 16)		5 30	20 200		5 30	20 200		5 30	20 200	ps
<sup>t</sup> JITTER	$\begin{array}{ll} \text{RMS Random Clock Jitter (Note 14)} & f_{in} = 1.0 \text{ GHz} \\ f_{in} = 1.5 \text{ GHz} \\ \text{Deterministic Jitter (Note 15)} & f_{DATA} = 622 \text{ Mb/s} \\ f_{DATA} = 1.5 \text{ Gb/s} \\ f_{DATA} = 2.488 \text{ Gb/s} \end{array}$		0.5 0.5 6.0 7.0 10	1.0 1.0 20 20 20		0.5 0.5 6.0 7.0 10	1.0 1.0 20 20 20		0.5 0.5 6.0 7.0 10	1.0 1.0 20 20 20	ps
V <sub>INPP</sub>	Input Voltage Swing/Sensitivity (Differential Configuration) (Note 13)	100		V <sub>CC</sub> - GND	100		V <sub>CC</sub> - GND	100		V <sub>CC</sub> - GND	mV
t <sub>r</sub> t <sub>f</sub>	Output Rise/Fall Times @ 250 MHz Q, Q (20% - 80%)	60	120	190	60	120	190	60	120	190	ps

#### Table 6. AC CHARACTERISTICS $V_{CC}$ = 3.0 V to 3.6 V, GND = 0 V; (Note 12)

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

12. Measured by forcing V<sub>INPPmin</sub> with 50% duty cycle clock source and V<sub>CC</sub> – 1400 mV offset. All loading with an external  $R_L = 100 \Omega$ . Input edge rates 150 ps (20%–80%). See Figure 17.

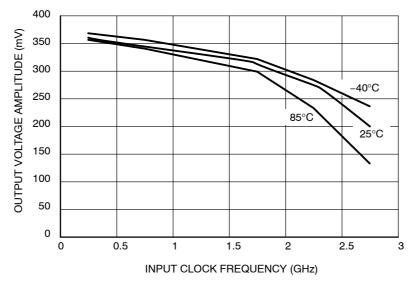
13. Input voltage swing is a single-ended measurement operating in differential mode.

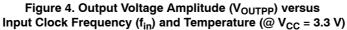
14. RMS jitter with 50% Duty Cycle clock signal at 750 MHz.

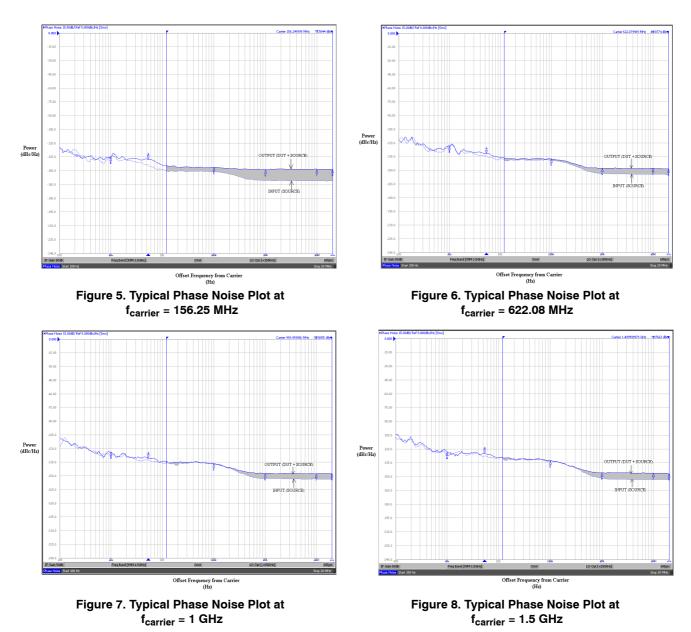
15. Deterministic jitter with input NRZ data at PRBS 223-1 and K28.5.

16. Skew is measured between outputs under identical transition @ 250 MHz.

17. The worst case condition between  $Q0/\overline{Q0}$  and  $Q1/\overline{Q1}$  from either  $D0/\overline{D0}$  or  $D1/\overline{D1}$ , when both outputs have the same transition.







The above phase noise plots captured using Agilent E5052A show additive phase noise of the NB6N14S device at frequencies 156.25 MHz, 622.08 MHz, 1 GHz and 1.5 GHz respectively at an operating voltage of 3.3 V in room temperature. The RMS Phase Jitter contributed by the

device (integrated between 12 kHz and 20 MHz; as shown in the shaded region of the plot) at each of the frequencies is 182 fs, 31 fs, 20 fs and 15 fs respectively. The input source used for the phase noise measurements is Agilent E8663B.



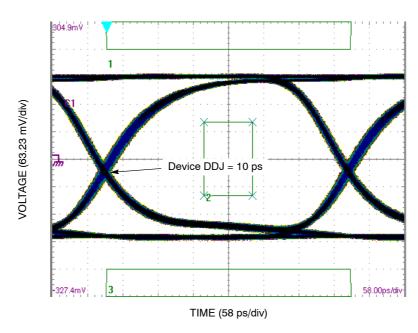
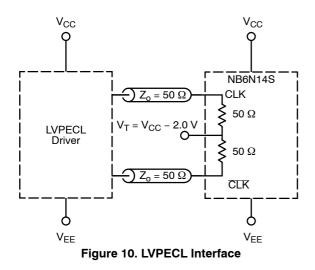


Figure 9. Typical Output Waveform at 2.488 Gb/s with PRBS  $2^{23-1}$  and OC48 mask (V\_{INPP} = 100 mV; Input Signal DDJ = 14 ps)



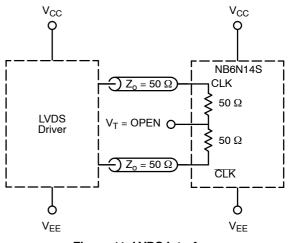


Figure 11. LVDS Interface

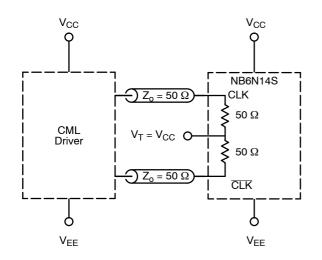
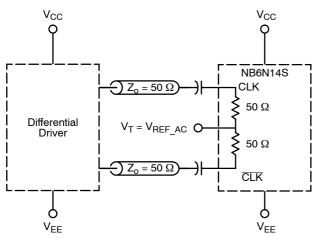


Figure 12. Standard 50  $\Omega$  Load CML Interface





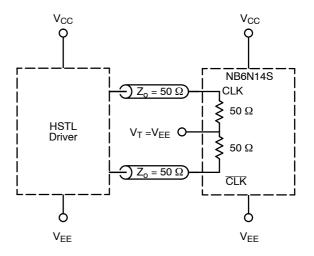
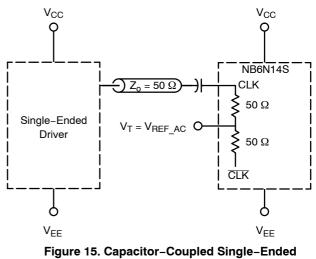
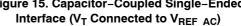
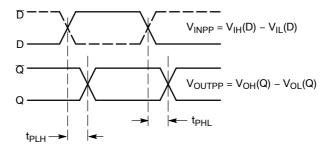


Figure 13. Standard 50  $\Omega$  Load HSTL Interface









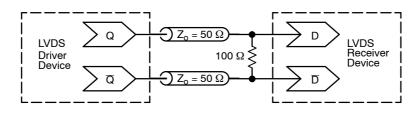
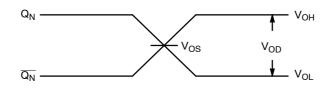
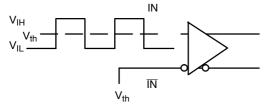
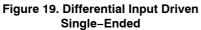


Figure 17. Typical LVDS Termination for Output Driver and Device Evaluation









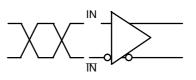


Figure 20. Differential Inputs Driven Differentially

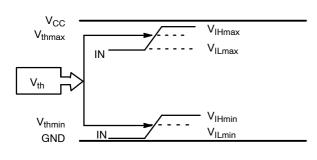


Figure 21. V<sub>th</sub> Diagram

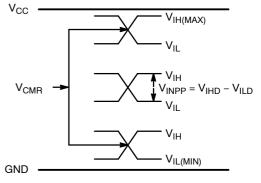


Figure 22. V<sub>CMR</sub> Diagram

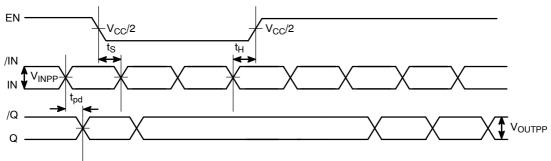


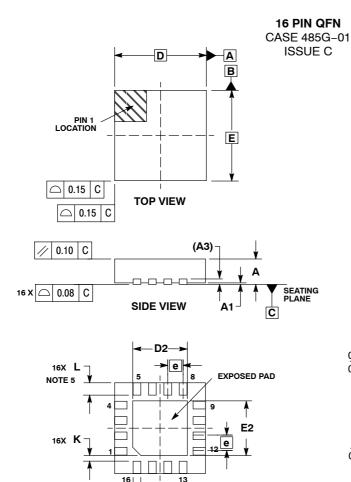
Figure 23. EN Timing Diagram

#### **ORDERING INFORMATION**

Device	Package	Shipping <sup>†</sup>
NB6N14SMNG	QFN-16, 3 X 3 mm (Pb-Free)	123 Units / Rail
NB6N14SMNR2G	QFN–16, 3 X 3 mm (Pb–Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

#### PACKAGE DIMENSIONS



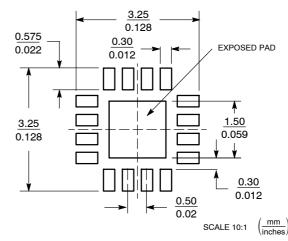
**BOTTOM VIEW** 

NOTES

- DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
- CONTROLLING DIMENSION: MILLIMETERS. DIMENSION 6 APPLIES TO PLATED 2 З. TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
- 0.23 AND 0.30 MM FROM TERMINAL. COPLANATITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.  $L_{max}$  CONDITION CAN NOT VIOLATE 0.2 MM MINIMUM SPACING BETWEEN LEAD TIP 5. AND FLAG

	MILLIMETERS					
DIM	MIN	MAX				
Α	0.80	1.00				
A1	0.00	0.05				
A3	0.20 REF					
b	0.18	0.30				
D	3.00 BSC					
D2	1.65	1.85				
Е	3.00	BSC				
E2	1.65	1.85				
е	0.50	BSC				
κ	0.18 TYP					
L	0.30	0.50				

#### **SOLDERING FOOTPRINT\***



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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